IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

(Attorney Docket No. 16106US02)

In the Application of:

Frederic Hayem, et al.

Serial No. 10/733,856

Filed: December 11, 2003

For: SYNCHRONIZATION OF MULTIPLE PROCESSORS IN A MULTI-MODE WIRELESS COMMUNICATION DEVICE

Examiner: Fred A. Casca

Group Art Unit: 2617

Confirmation No. 8105

Electronically Filed on August 31, 2009

REVISED APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Revised Appeal Brief supersedes the Appeal Brief, which was filed on July 6, 2009. The Appellant notes that this Revised Appeal Brief is timely filed within the period for reply that ends on September 6, 2009

This is an appeal from an Office Action mailed on December 11, 2008 ("Final Office Action"), in which claims 1-43 were finally rejected. The Appellant respectfully requests

that the Board of Patent Appeals and Interferences ("Board") reverse the final rejection of claims 1-43 of the present application.

REAL PARTY IN INTEREST
(37 C.F.R. § 41.37(c)(1)(i))

Broadcom Corporation, a corporation organized under the laws of the state of California, and having a place of business at 5300 California Avenue, Irvine, California 92617, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment recorded at Reel 015247, Frame 0903 and Reel 015349, Frame 0953 in the PTO Assignment Search room.

RELATED APPEALS AND INTERFERENCES
(37 C.F.R. § 41.37(c)(1)(ii))

The Appellant is unaware of any related appeals or interferences.

STATUS OF THE CLAIMS
(37 C.F.R. § 41.37(c)(1)(iii))

Claims 1-43 were finally rejected. Pending claims 1-43 are the subject of this appeal. Claims 2-8, 10-14, 16-19, 21-27, 29-33, 35-37 and 39-43 depend directly or indirectly from independent claims 1, 9, 15, 20, 28, 34 and 38, respectively.

Claims 6, 7, 13, 16, 25, 26, 32, 36, 41, and 42 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement.

Claims 1-5, 8-12, 14-18, 20-24, and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over USPP 2002/0141441 ("Neumann"), in view of USP 5,918,040 ("Jarvis").

Claims 6, 13, 19, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Neumann, in view of Jarvis, and further in view of MPEP 2144.03.

Claims 7 and 26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Neumann, in view of Jarvis, further in view of MPEP 2144.03, and still further in view of USPP 2002/0186754 ("Kawai").

Claims 28-43 are rejected for the same rationale as used for claims 1-27.

The Appellant identifies claims 1-43 as the claims that are being appealed. The text of the pending claims is provided in the Claims Appendix.

STATUS OF AMENDMENTS
(37 C.F.R. § 41.37(c)(1)(iv))

The Appellant has not amended any claims subsequent to the final rejection of claims 1-43 mailed on December 11, 2008.

SUMMARY OF CLAIMED SUBJECT MATTER
(37 C.F.R. § 41.37(c)(1)(v))

The invention of claim 1 is illustratively described in, for example, the "Summary

of the Invention" at page 5, and at least the detail descriptions of Figs. 9-13. For example, the present invention relates in one aspect to a multi-mode wireless communication device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10) comprised of multiple synchronized processors. *See* present application at page 5, lines 5-6. In particular, the wireless device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10) includes a host baseband processor (e.g. host GSM/GPRS baseband processor 1001 in Fig. 10) configured to operate in accordance with a first wireless communications protocol of a first wireless communications system (e.g. GSM wireless communications system). *See id* at page 5, lines 6-8. The device further includes a baseband co-processor (WCDMA baseband co-processor 1004 in Fig. 10) configured to operate in accordance with a second wireless communications protocol of a second wireless communications system (WCDMA wireless communications system). *See id* at page 5, lines 9-11. A synchronization arrangement is provided for establishing timing synchronization (e.g. via sample counter 1104 and slot counter 1108 in Fig. 11 consistent with the GSM and WCDMA protocols) between the first and second wireless communications systems (e.g. the respective GSM and WCDMA wireless communication systems) within the device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10) on the basis of timing information transferred (e.g. reading of the values of sample counter 1104 and slot counter 1108 in Figs. 12 and 13) to the host

baseband processor (e.g. host GSM/GPRS baseband processor 1001 in Fig. 10) from the baseband co-processor (WCDMA baseband co-processor 1004 in Fig. 10). See id at page 5, lines 11-14.

Claims 2-8 are dependent directly or indirectly upon independent claim 1.

The invention of claim 9 is illustratively described in, for example, the "Summary of the Invention" at page 5, and at least the detail descriptions of Figs. 9-13. For example, in another aspect, the invention relates to a method for effecting timing synchronization within a multi-mode communication device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10). *See id* at page 5, lines 20-21. The method includes configuring a host baseband processor (e.g. host GSM/GPRS baseband processor 1001 in Fig. 10) of the communication device to operate in accordance with a first wireless communications protocol of a first wireless communications system (e.g. GSM wireless communications system). *See id* at page 5, lines 21-24. A baseband co-processor (WCDMA baseband co-processor 1004 in Fig. 10) within the device is also configured to operate in accordance with a second wireless communications protocol of a second wireless communications system (WCDMA wireless communications system). *See id* at page 5, lines 24-26. The method includes establishing, within the device, timing synchronization (i.e., determining a timing relationship between the first and second wireless communication systems) between the first and second communication systems on the

basis of timing information (e.g. reading of the values of sample counter 1104 and slot counter 1108 in Figs. 12 and 13) transferred to the host baseband processor (e.g. host GSM/GPRS baseband processor 1001 in Fig. 10) from the baseband coprocessor (WCDMA baseband co-processor 1004 in Fig. 10). *See id* at page 5, lines 26-29.

Claims 10-14 are dependent directly or indirectly upon independent claim 9.

The invention of claim 15 is illustratively described in, for example, the "Summary of the Invention" at page 6, and at least the detail descriptions of Figs. 9-13. For example, the present invention also pertains to a method for effecting timing synchronization between a first wireless communication system and a second wireless communication system (e.g. GSM and WCDMA wireless communications system) within a multi-mode communication device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10). *See id* at page 6, lines 3-5. The method includes generating a timer capture interrupt (e.g. GSM interrupt pulse 1310 in Fig. 13) during a predetermined timing phase (e.g. the GSM interrupt pulse 1310 executed at a predetermined GSM clock cycle (GSM clk) in Fig. 13) of the first wireless communication system (e.g. GSM wireless communications system). *See id* at page 6, lines 5-7. A timer value (e.g. WCDMA counter value slot_cnt in Fig. 13) of at least one timer (e.g. WCDMA slot counter 1108 in Fig. 11) pertinent to operation of the second wireless communication system (e.g. WCDMA wireless communications system) is stored (i.e., in the various registers of the WCDMA

baseband co-processor 1004 in Fig. 10) space in response to the timer capture interrupt (e.g. GSM interrupt pulse 1310 in Fig. 13). *See id* at page 6, lines 7-9. The method further includes reading the timer value (e.g. WCDMA counter value slot_cnt in Fig. 13) and determining a timing relationship between the first and second wireless communication systems (e.g. GSM and WCDMA wireless communications system) based upon the timer value (e.g. WCDMA counter value slot_cnt in Fig. 13).

Claims 16-19 are dependent directly or indirectly upon independent claim 15.

The invention of claim 20 is illustratively described in, for example, "Summary of the Invention" at page 5, and at least the detail descriptions of Figs. 9-13. For example, the present invention relates in one aspect to a multi-mode wireless communication device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10) comprised of multiple synchronized processors. *See id* at page 5, lines 5-6. In particular, the wireless device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10) includes a host baseband processor (e.g. host GSM/GPRS baseband processor 1001 in Fig. 10) configured to operate in accordance with a first wireless communications protocol of a first wireless communications system (e.g. GSM wireless communications system). *See id* at page 5, lines 6-8. The device further includes a baseband co-processor (WCDMA baseband co-processor 1004 in Fig. 10) configured to operate in accordance with a second wireless communications protocol of

a second wireless communications system (WCDMA wireless communications system). *See id* at page 5, lines 9-11. A synchronization arrangement is provided for establishing timing synchronization (e.g. via WCDMA sample counter 1104 and WCDMA slot counter 1108 in Fig. 11 consistent with the GSM and WCDMA protocols) between the first and second wireless communications systems (e.g. the respective GSM and WCDMA wireless communication systems) within the device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10) on the basis of timing information transferred (e.g. reading of the values of WCDMA sample counter 1104 and WCDMA slot counter 1108 in Figs. 12 and 13) to the host baseband processor (e.g. host GSM/GPRS baseband processor 1001 in Fig. 10) from the baseband co-processor (WCDMA baseband co-processor 1004 in Fig. 10). *See id* at page 5, lines 11-14. In addition, Fig. 10 discloses that the baseband co-processor (e.g. WCDMA baseband co-processor 1004 in Fig. 10) and/or additional circuitry (e.g. baseband interface 1022 and resyn pulse generator 1320 in Fig. 10) may also enable timing synchronization between the first and second wireless communication systems on the basis of timing information transferred to the host baseband processor from the baseband co-processor.

Claims 21-27 are dependent directly or indirectly upon independent claim 20.

The invention of claim 28 is illustratively described in, for example, "Summary of the Invention" at page 5, and at least the detail descriptions of Figs. 9-13. For example,

the present invention relates in one aspect to a multi-mode wireless communication device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10) comprised of multiple synchronized processors. *See id* at page 5, lines 5-6. In particular, the wireless device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10) includes a host baseband processor (e.g. host GSM/GPRS baseband processor 1001 in Fig. 10) configured to operate in accordance with a first wireless communications protocol of a first wireless communications system (e.g. GSM wireless communications system). *See id* at page 5, lines 6-8. The device further includes a baseband co-processor (WCDMA baseband co-processor 1004 in Fig. 10) configured to operate in accordance with a second wireless communications protocol of a second wireless communications system (WCDMA wireless communications system). *See id* at page 5, lines 9-11. A synchronization arrangement is provided for establishing timing synchronization (e.g. via WCDMA sample counter 1104 and WCDMA slot counter 1108 in Fig. 11 consistent with the GSM and WCDMA protocols) between the first and second wireless communications systems (e.g. the respective GSM and WCDMA wireless communication systems) within the device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10) on the basis of timing information transferred (e.g. reading of the values of WCDMA sample counter 1104 and WCDMA slot counter 1108 in Figs. 12 and 13) to the host baseband processor (e.g. host GSM/GPRS baseband processor

1001 in Fig. 10) from the baseband co-processor (WCDMA baseband co-processor 1004 in Fig. 10). *See id* at page 5, lines 11-14. In addition, the specification at page 20, lines 7-21 supports the claim language "said establishing includes issuing a timer capture interrupt (e.g. GSM interrupt pulse 1310 in Figs. 10 and 13) to said baseband co-processor (WCDMA baseband co-processor 1004 in Fig. 10), and wherein said establishing comprises providing at least one timer value (e.g. WCDMA counter value slot_cnt in Fig. 13) pertinent to a timing state of said second wireless communications system (e.g. WCDMA wireless communication system) to said host baseband processor (e.g. host GSM/GPRS baseband processor 1001 in Fig. 10) in response to issuance of said timer capture interrupt (e.g. GSM interrupt pulse 1310 in Figs. 10 and 13)."

The invention of claim 34 is illustratively described in, for example, the "Summary of the Invention" at page 5, and at least the detail descriptions of Figs. 9-13. For example, in another aspect, the invention relates to a method for effecting timing synchronization within a multi-mode communication device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10). *See id* at page 5, lines 20-21. The method includes configuring a host baseband processor (e.g. host GSM/GPRS baseband processor 1001 in Fig. 10) of the communication device to operate in accordance with a first wireless communications protocol of a first wireless communications system (e.g. GSM wireless communications system). *See id* at page 5, lines 21-24. A baseband co-processor (WCDMA baseband co-processor 1004 in Fig. 10) within the device is also configured to operate in

accordance with a second wireless communications protocol of a second wireless communications system (WCDMA wireless communications system). *See id* at page 5, lines 24-26. The method includes establishing, within the device, timing synchronization (i.e., determining a timing relationship between the first and second wireless communication systems) between the first and second communication systems on the basis of timing information (e.g. reading of the values of sample counter 1104 and slot counter 1108 in Figs. 12 and 13) transferred to the host baseband processor (e.g. host GSM/GPRS baseband processor 1001 in Fig. 10) from the baseband coprocessor (WCDMA baseband co-processor 1004 in Fig. 10). *See id* at page 5, lines 26-29. In certain implementations establishing such timing synchronization (i.e., determining a timing relationship between the first and second wireless communication systems) may include issuing a timer capture interrupt (e.g. Timer Capture Interrupt 1310 in Fig. 10) to the baseband co-processor (WCDMA baseband co-processor 1004 in Fig. 10). *See id* at page 5, lines 29-30. In response, the baseband co-processor provides at least one timer value pertinent to a timing state of the second wireless communications protocol to the baseband processor (e.g. reading of the values of WCDMA sample counter 1104 and WCDMA slot counter 1108 in Figs. 12 and 13). *See id* at page 6, lines 1-2.

Claims 35-37 are dependent directly or indirectly upon independent claim 34.

The invention of claim 38 is illustratively described in, for example, "Summary of the Invention" at page 5, and at least the detail descriptions of Figs. 9-13. For example,

the present invention relates in one aspect to a multi-mode wireless communication device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10) comprised of multiple synchronized processors. *See id* at page 5, lines 5-6. In particular, the wireless device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10) includes a host baseband processor (e.g. host GSM/GPRS baseband processor 1001 in Fig. 10) configured to operate in accordance with a first wireless communications protocol of a first wireless communications system (e.g. GSM wireless communications system). *See id* at page 5, lines 6-8. The device further includes a baseband co-processor (WCDMA baseband co-processor 1004 in Fig. 10) configured to operate in accordance with a second wireless communications protocol of a second wireless communications system (WCDMA wireless communications system). *See id* at page 5, lines 9-11. A synchronization arrangement is provided for establishing timing synchronization (e.g. via WCDMA sample counter 1104 and WCDMA slot counter 1108 in Fig. 11 consistent with the GSM and WCDMA protocols) between the first and second wireless communications systems (e.g. the respective GSM and WCDMA wireless communication systems) within the device (e.g. tri-mode wireless terminal platform 900 in Fig. 9 and dual mode wireless terminal baseband platform 1000 in Fig. 10) on the basis of timing information transferred (e.g. reading of the values of WCDMA sample counter 1104 and WCDMA slot counter 1108 in Figs. 12 and 13) to the host baseband processor (e.g. host GSM/GPRS baseband processor

1001 in Fig. 10) from the baseband co-processor (WCDMA baseband co-processor 1004 in Fig. 10). *See* id at page 5, lines 11-14. In addition, Fig. 10 discloses that the baseband co-processor (e.g. WCDMA baseband co-processor 1004 in Fig. 10) and/or additional circuitry (e.g. baseband interface 1022 and resyn pulse generator 1320 in Fig. 10) may issue, from the host baseband processor (e.g. host GSM/GPRS baseband processor 1001 in Fig. 10), a timer capture interrupt (e.g. GSM interrupt pulse 1310 in Figs. 10 and 13) to the baseband co-processor (WCDMA baseband co-processor 1004 in Fig. 10) during a predetermined timer phase (e.g. the GSM interrupt pulse 1310 executed at a predetermined GSM clock cycle (GSM clk) in Fig. 13) of the first wireless communications system (GSM wireless communication system). In addition, Figs. 10-13 discloses that the claim language "said one or more of said host baseband processor (e.g. host GSM/GPRS baseband processor 1001 in Fig. 10), said baseband co-processor (WCDMA baseband co-processor 1004 in Fig. 10) and/or the additional circuitry (e.g. baseband interface 1022 and resyn pulse generator 1320 in Fig. 10) is configured to provide at least one timer value (e.g. WCDMA counter value slot_cnt in Fig. 13) pertinent to a timing state of said second wireless communications system (e.g. WCDMA wireless communication system) in response to issuance of said timer capture interrupt (e.g. GSM interrupt pulse 1310 in Figs. 10 and 13), the one or more of said host baseband processor, the baseband co-processor and/or said additional circuitry enables determining of a timing difference between the first and second wireless communication systems based upon the predetermined timer phase (e.g. the GSM

interrupt pulse 1310 executed at a predetermined GSM clock cycle (GSM clk) in Fig. 13) and the at least one timer value (e.g. WCDMA counter value slot_cnt in Fig. 13)."

Claims 39-43 are dependent directly or indirectly upon independent claim 38.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. § 41.37(c)(1)(vi))

Claims 6, 7, 13, 16, 25, 26, 32, 36, 41, and 42 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement.

Claims 1-5, 8-12, 14-18, 20-24, and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Neumann, in view of Jarvis.

Claims 6, 13, 19, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Neumann, in view of Jarvis, and further in view of MPEP 2144.03.

Claims 7 and 26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Neumann, in view of Jarvis, further in view of MPEP 2144.03, and still further in view of Kawai.

Claims 28-43 are rejected for the same rationale as used for claims 1-27.

ARGUMENT
(37 C.F.R. § 41.37(c)(1)(vii))

I. REJECTION UNDER 35 U.S.C. § 112

Claims 6, 7, 13, 16, 25, 26, 32, 36, 41, and 42 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement. Specifically, the Examiner requests further explanation of how the "**additional** timer value" pertains to the "**second** wireless communication protocol" in Appellant's Figs. 10-13.

The Examiner is referred to the description of Appellant's Fig. 10:

> "The WCDMA baseband co-processor 1004 further includes **a master timer 1018 configured to maintain counter values utilized by the WCDMA modem 1016**. The **WCDMA baseband co-processor 1004 operates to perform physical layer processing of WCDMA bearer signals**, and interfaces with the host baseband processor 1001 through a baseband interface 1022."

See Appellant's Fig. 10 and Specification at page 18, lines 10-16. Appellant's Fig. 10 discloses that the WCDMA baseband co-processor 1004 has a WCDMA master timer 1018, which maintains counter values (i.e., timer values) to be utilized by the WCDMA modem 1016. Since the physical layer processing functions of the WCDMA bearer signals (i.e., of the second wireless communication protocol) are carried out by the WCDMA baseband co-processor 1004, therefore, the counter values (i.e., timer values) of the WCDMA master timer 1018 are pertinent to the second wireless communication protocol.

The Examiner is also referred to the description in Appellant's Fig. 11, which states:

"Turning now to FIG. 11, ...a **counter 1100 maintained by the WCDMA**

> **master timer 1018** of the WCDMA baseband coprocessor 1004. The **counter 1100 includes two fields**; namely, **a sample counter 1104 and slot counter 1108**. In the exemplary embodiment **both of the counters 1104 and 1108 are free-running at every rising edge of the 15.36 MHz system clock** (not shown) of the WCDMA baseband co-processor 1004."

See Appellant's Fig. 11 and Specification at page 19, lines 24-29. Appellant's Fig. 11 likewise discloses that **the counter 1100** maintained by the WCDMA master timer, is **a two field counter**, including "**a sample counter 1104 and slot counter 1108**". In other words, the Appellant discloses that **there are two different counter values (i.e., timer values) that pertain to the second wireless protocol communication**. Since the sample counter 1104 and the slot counter 1108 are both clocked (or timed) to the rising edge of the system clock of the WCDMA baseband co-processor 1004, consequently, the counter values of the sample counter 1104 and the slot counter 1108 are both timer values, that pertain to the WCDMA protocol (i.e., the second wireless communication protocol). In this regard, Appellant's Figs. 10-11 and their related description in the specification support the notion that the "**additional timer value**" pertains to the "**second wireless communication protocol**," as recited in Appellant's claim 6.

Furthermore, Appellant's Figs. 10-11 also support Appellant's claim 7, which recites "said at least one timer value corresponds to a slot counter and said additional timer value corresponds to a sample counter." Moreover, Appellant's Figs. 12-13 disclose that both the timing values of the sample_cnt 1104 (i.e., the additional timer value) and the slot_cnt 1108 (i.e., the one timer value), are clocked at the rising edges

of the WCDMA system clock (15.36 MHz) in the second wireless protocol communication. Accordingly, claim 7 clarifies both the "one timer value" and the "additional timer value", as recited in claim 6.

Based on the above explanation, the Appellant maintains that claims 6, 7, 13, 16, 25, 26, 32, 36, 41, and 42 are fully supported by Appellant's Figs. 10-13 and the related description, and respectfully request that the rejection under 35 U.S.C. § 112, first paragraph be withdrawn.

II. REJECTION UNDER 35 U.S.C. § 103

In order for a *prima facie* case of obviousness to be established, the Manual of Patent Examining Procedure, Rev. 6, Sep. 2007 ("MPEP") states the following:

> The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385, 1396 (2007) noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Federal Circuit has stated that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."

See the MPEP at § 2142, citing *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006), and *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d at 1396 (quoting Federal Circuit statement with approval). Further, MPEP § 2143.01 states that "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the results would have been predictable to one of

ordinary skill in the art" (citing *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396 (2007)). Additionally, if a *prima facie* case of obviousness is not established, the Appellant is under no obligation to submit evidence of nonobviousness:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the Appellant is under no obligation to submit evidence of nonobviousness.

See MPEP at § 2142.

A. The Proposed Combination of Neumann and Jarvis Does Not Render Claims 1-5, 8-12, 14-18, 20-24, and 27 Unpatentable

The Appellant now turns to the rejection of claims 1-5, 8-12, 14-18, 20-24, and 27 as being unpatentable over Neumann in view of Jarvis.

A(1). Independent Claims 1, 9 and 20

Regarding claim 1, the Appellant maintains that the combination of Jarvis and Neumann does not disclose "said host baseband processor enables timing synchronization between said **first and second wireless communications systems** on the basis of timing information transferred to said host baseband processor form said baseband co-processor," as recited in Appellant's claim 1.

The Examiner concedes the following:

> "Neumann does not specifically disclose the host baseband processor enabling timing synchronization between the first and second wireless communication systems on the basis of timing information transferred to

> the host baseband processor from the baseband co-processor as claimed."

See the Final Office Action in page 3. The Examiner looks to Jarvis to disclose Neumann's deficiencies, and states the following:

> "Jarvis discloses a processor enabling timing synchronization **between two network systems** on the basis of timing information sent from another processor (Figures 1-5b, abstract, col. 2, lines 7-21 and 45-65, col. 3, and lines 35-67)."

See the Final Office Action in page 3. The Appellant points out that Jarvis in Fig. 1 discloses an optical network 13 and an Ethernet network 15, where neither network systems pertains to a first or second "**wireless** communication system," as recited in Appellant's claim 1. In this regard, the Appellant submits that Jarvis is not a combinable reference to Neumann.

In addition, Jarvis in Fig. 1 discloses a line card 12, which communicates with the optical network 13, and a line card 14, which communicates with the Ethernet network 15. Jarvis also discloses that the line card 12 in the optical network 13 has two processors, namely, an interface 30 (timed by a timer 31), and a packet processor 32 (timed by a timer 32). Jarvis discloses a timer synchronization operation, where the interface 30 or the packet processor 32 could operate as either a master processor with a master timer, or a slave processor with a slave timer, respectively.

Likewise, Jarvis in Fig. 1 discloses that the line card 14 in the Ethernet network 15 has two processors, namely, an interface 30 (timed by a timer 31), and a packet

processor 32 (timed by a timer 32), where the interface 30 or the packet processor 32 could operate as either a master processor with a master timer, or a slave processor with a slave timer, respectively.

In effect, the Examiner equates one of Jarvis' processors, i.e., the interface 30 or the packet processor 32, to Appellant's host baseband processor. The Examiner also equates one of Jarvis' processors, i.e., the interface 30 or the packet processor 32, to Appellant's baseband co-processor.

Jarvis names the processors 30, 32 and respective timers 31, 33 of line card 12 in the optical network 13 to be the same as the processors 30, 32 and respective timers 31, 33 of line card 14 in the Ethernet network 15. In this regard, it is unclear whether the Examiner alleges that time synchronization takes place between the processors 30, 32 and respective timers 31, 33, is between the respective line card 12 (in optical network 13) and line card 14 (in Ethernet network 15). It is equally unclear, whether the Examiner alleges that time synchronization takes place between the processors 30, 32 and timers 31, 33, is within the same line card, such as line card 12 (in optical network 13) or line card 14 (in Ethernet network 15).

Nevertheless, the Appellant has argued both positions in the 3/11/09 response to Final Office Action and in the 4/8/09 Pre-Appeal Brief. More specifically, the Appellant (in pages 22-23 of the 3/11/09 response to Final Office Action), argued that Jarvis discloses a time synchronization operation between the processors 30 and 32, which

takes place within the same device, i.e., within line card 12 in optical network 13, or within line card 14 in Ethernet network 15. In this regard, Jarvis does not disclose or suggest "said host baseband processor enables timing synchronization between said **first and second wireless communications systems** on the basis of timing information transferred to said host baseband processor form said baseband co-processor," as recited in claim 1.

In response, the Examiner in page 2 of the Advisory Action, argued the relevancy of Jarvis' line card 12 or 14, a feature that the Examiner did not cite to reject Appellant's claim 1. The Appellant respectfully disagrees with the Examiner's relevancy argument. In the Pre-Appeal Brief, the Appellant pointed out that Jarvis clearly discloses that whether the interface 30 (with timer 31) or the packet processor 32 (with timer 33) performs the **alleged** "**enabling of timing synchronization**", both processors (i.e., the interface 30 and packet processor 32) still process time stamped packets within the **same network**, namely, line card 12 in optical network system 13, or line card 14 in Ethernet network 15. In this regard, **Jarvis' alleged enabling timing synchronization does not take place between two different network systems**. Therefore, Jarvis does not disclose or suggest "said host baseband processor enables timing synchronization **between said first and second wireless communication systems** on the basis of timing information transferred to said host baseband processor from said baseband co-processor" as recited in Appellant's claim 1.

In addition, even assuming arguendo, that Jarvis discloses that the timing synchronization between the processors 30, 32 takes place between two different line cards, namely between line card 12 (in optical network 13) and line card 14 (in Ethernet network 15), the Examiner's argument is still deficient. More specifically, neither the optical network 13 nor the Ethernet network 15 is "a wireless communication system", as alleged by the Examiner.

Moreover, even assuming arguendo that Jarvis discloses that the alleged "enabling timing synchronization" takes place within the same device (within line card 12 or 14), qualifies as between two wireless communication systems (which it does not), the Examiner's argument is still deficient. For example, Jarvis clearly discloses an arbitrary timer value adjustment operation based on the comparison result. In other words, the alleged "enabling of timing synchronization" between the two timers 31 and 33 for respective processors 30 and 32, may take place in both directions (see Jarvis' Figs. 2-4b). For example, Jarvis discloses that both the master timer (31 or 33) and the slave timer (33 or 31) could increment its timer value (see Jarvis at the abstract and col. 4, lines 1-44) based on which timer value is higher. For example, the timing value of the master timer 31 in processor 30 (the alleged host baseband processor) may or may not increment, depending on whether the timing value of the slave timer 33 in processor 32 (the alleged baseband co-processor) is higher or lower than the timing value of the master timer 31. In other words, Jarvis discloses that the timer value adjustment (i.e., the alleged "enable timing synchronization") is bidirectional, and not in a single direction

(i.e., not on the basis of timing information **transferred to** said host baseband processor **from** said baseband co-processor).

Therefore, Jarvis's above disclosure refutes the Examiner's argument that Jarvis discloses or suggest "said host baseband processor enables timing synchronization between said first and second wireless communication systems on the basis of timing information transferred to said host baseband processor from said baseband co-processor," as recited in Appellant's claim 1. Neumann does not overcome Jarvis' above deficiencies, and the Appellant maintains that claim 1 is allowable.

Independent claims 9 and 20 are similar in many respects to the device disclosed in independent claim 1. Therefore, the Appellant submits that independent claims 9 and 20 are also allowable over the references cited in the Final Office Action at least for the reasons stated above with regard to claim 1.

B. Rejection of Independent Claim 15

With regard to the rejection of independent claim 15 under 35 U.S.C. § 103(a), the Appellant submits that the combination of Neumann and Jarvis does not disclose or suggest at least the limitation of "**generating within a multi-mode communication device**, **a timer capture interrupt during a predetermined timing phase** of a first wireless communication system," as recited by the Appellant in independent claim 15.

In regard to claim 15, the Final Office Action, at page 6, concedes the following:

> Neumann does not specifically discuss synchronization details e.g., generating a timer capture interrupt during a predetermined timing phase of a first wireless communication system, storing a timer value of at least one time pertinent to operation of the second wireless communication system in response to the timer capture interrupt; reading the timer value; and determining a timing relationship between the first and second wireless communication systems based upon the timer value in the format claimed by applicant.

The Examiner then relies on Jarvis for the deficiencies of Neumann, and states the following:

> Jarvis discloses generating a timer capture interrupt during a predetermined timing phase of a first communication system (Figures 2-5b and col. 3, lines 59-63, col. 4, lines 1-44, col. 5, lines 1-16, "master M issues to the slave S, a data packet containing a synchronization request and its current time value Mo"), storing a timer value of at least one time pertinent to operation of said second wireless communication system in response to said timer capture interrupt (Figures 2-5b, col. 3, lines 64-67, col. 4, lines 1-44, col. 5, lines 1-16, "So"); reading said timer value (Figures 2-5b, col. 3, lines 64-67, col. 4, lines 1-44, col. 5, lines 1-16, "compares the issued master time value", note that comparing implies reading); and **determining a timing relationship between said first and second wireless communication systems based upon said timer value** (Figures 2-5b, col. 3, lines 64-67, col. 4, lines 1-44, col. 5, lines 1-16).

See id. (emphasis added). The Examiner in the Final Office Action argued that "a person of ordinary skill in the art would know how the generating of timing capture would be applied to the multimode communication device of Neumann/Jarvis". The Appellant respectfully disagrees, since neither Neumann nor Jarvis disclose or suggest "**generating**

…, **a timer capture interrupt** during a predetermined timing phase", let alone disclose or suggest the claimed "**generating within a multi-mode communication device**,… **during a predetermined timing phase**".

In page 2 of the Advisory Action, the Examiner argued that Jarvis does not need to disclose "generating a timer capture interrupt during a predetermined timing phase". The Examiner reasoned that during a timing synchronizing process, different timing values need to be received and captured to perform comparison and adjustment.

However, the Appellant did not argue that Jarvis does not disclose receiving or capturing of different timing values. Instead, the Appellant argued that "**generating a timer capture interrupt**" is not disclosed (*see* 3/11/09 response in pages 25-26). For example, the direct access read operation disclosed in Appellant's Fig. 12 also reads (i.e., receives and captures) the timer values of the sample counter and slot counter. Appellant's Fig. 13 specifically discloses generating an interrupt pulse 1310 by the host GSM processor using a GSM clk at a predetermined timing phase. However, **Jarvis clearly does not disclose such interrupt pulse generation**, let alone **a predetermined timing phase**, as alleged by the Examiner. In this regard, the Examiner's allegation that it is customary in the art for receiving and capturing timing values to have "generating a timer capture interrupt during a predetermined timing phase" is unsupported.

Furthermore, the Appellant also argued that Jarvis also does not disclose "**storing a timer value** ...in response to the timer capture interrupt..." Moreover, the Appellant maintained that Jarvis' optical or Ethernet networks are not a "wireless communication network". Neumann does not overcome Jarvis' deficiencies, and the Appellant maintains that claim 15 is allowable.

Therefore, the combination of Neumann and Jarvis does not establish a prima facie case of obviousness to reject Appellant's claims 1, 9, 15 and 20 under 35 U.S.C. § 103(a), and should be allowable.

C. Rejection of Dependent Claims 4-5, 8, 10-12, 14, 16-18, 21-24, and 27

Based on at least the foregoing, the Appellant believes the rejection of independent claims 1, 9, 15, and 20 under 35 U.S.C. § 103(a) as being unpatentable over Neumann in view of Jarvis has been overcome and requests that the rejection be withdrawn. Claims 4-5, 8, 10-12, 14, 16-18, 21-24, and 27 depend from independent claims 1, 9, 15, and 20, respectively, and are also respectfully submitted to be allowable.

In addition, with regard to the rejection of claim 2, the Appellant refers the Examiner to the arguments in claim 15, that neither Neumann nor Jarvis discloses "a timer capture interrupt to said baseband co-processor during a predetermined timer phase of said first wireless communications system," as recited in Appellant's claim 2.

Claim 2 is submitted to be allowable. Likewise, claims 10, 16 and 21 are similar in many respects to claim 2, and are submitted to be allowable for the same rationale of claim 2.

The Appellant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 4-5, 8, 10-12, 14, 16-18, 21-24, and 27.

IV. Rejection to Claims 6, 13, 19, and 25

Claims 6, 13, 19, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Neumann, in view of Jarvis, and further in view of MPEP 2144.03. Based on at least the foregoing, the Appellant believes the rejection of independent claims 1, 9, 15 and 20 under 35 U.S.C. § 103(a) has been overcome and requests that the rejection be withdrawn. MPEP 2144.03 does not overcome the deficiencies of Neumann and Jarvis, claims 6, 13, 19, and 25 depend from independent claims 1, 9, 15, and 20, respectively, and are, consequently, also respectfully submitted to be allowable.

In addition, with regard to the rejection of claim 6, the Appellant submits that neither Neumann nor Jarvis discloses "said baseband co-processor including first and second registers adapted to store said at least one timer value and an additional timer value pertinent to said second wireless communications protocol," as recited in Appellant's claim 6. Claim 6 is submitted to be allowable. Likewise, claims 13 and 25

are similar in many respects to claim 6, and are submitted to be allowable for the same rationale of claim 6.

The Appellant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 6, 13, 19, and 25.

V. Rejection to Claims 7 and 26

Claims 7 and 26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Neumann, in view of Jarvis, and further in view of MPEP 2144.03 and Kawai. Based on at least the foregoing, the Appellant believes the rejection of independent claims 1, 9, 15 and 20 under 35 U.S.C. § 103(a) has been overcome and requests that the rejection be withdrawn.

Additionally, MPEP 2144.03 and Kawai do not overcome the deficiencies of Neumann and Jarvis, claims 7 and 26 depend from independent claims 1 and 20, respectively, and are, consequently, also respectfully submitted to be allowable.

The Appellant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 7 and 26.

VI. Rejection to Claims 28-43

Claims 28-43 are rejected for the same rationale as used for claims 1-27. Since the Examiner has not provided any additional arguments for the rejection of claims 28-43, the Appellant submits that these claims are allowable at least for the reasons stated above regarding the allowability of claims 1-27.

The Appellant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 1-43.

CONCLUSION

For at least the foregoing reasons, the Appellant submits that claims 1-43 are not unpatentable by the combination of Neumann, Jarvis and Kawai. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Respectfully submitted,

Date: August 31, 2009

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CLAIMS APPENDIX
(37 C.F.R. § 41.37(c)(1)(viii))

1. A multi-mode wireless communication device, comprising:

a host baseband processor configured to operate in accordance with a first wireless communications protocol of a first wireless communications system; and

a baseband co-processor configured to operate in accordance with a second wireless communications protocol of a second wireless communications system,

wherein said host baseband processor enables timing synchronization between said first and second wireless communications systems on the basis of timing information transferred to said host baseband processor from said baseband co-processor.

2. The multi-mode communications device of claim 1, wherein said host baseband processor comprises circuitry for issuing, from said host baseband processor, a timer capture interrupt to said baseband co-processor during a predetermined timer phase of said first wireless communications system.

3. The multi-mode communication device of claim 2, wherein said baseband co-processor is configured to provide at least one timer value pertinent to a timing state of said second wireless communications system to said host baseband processor in response to issuance of said timer capture interrupt, said host baseband processor enables determining of a timing difference between said first and second wireless

communication systems based upon said predetermined timer phase and said at least one timer value.

4. The multi-mode communications device of claim 1, wherein said host baseband processor comprises circuitry for reading a current value of at least one timer maintained by said baseband co-processor consistent with said second wireless communications protocol.

5. The multi-mode communications device of claim 1, wherein said host baseband processor comprises a higher-layer processing module and a modem for interfacing with said first wireless communication system, said higher-layer processing module being operatively coupled to said modem and to a baseband interface of said baseband co-processor.

6. The multi-mode communications device of claim 3, wherein said second wireless communications protocol comprises WCDMA, said baseband co-processor including first and second registers adapted to store said at least one timer value and an additional timer value pertinent to said second wireless communications protocol.

7. The multi-mode communications device of claim 6, wherein said at least one timer value corresponds to a slot counter and said additional timer value corresponds to a sample counter.

8. The multi-mode communications device of claim 1, wherein said host baseband processor comprises a higher-layer processor configured to effect higher-layer processing of information processed by said baseband co-processor.

9. A timing synchronization method, comprising:

configuring a host baseband processor of a multi-mode device to operate in accordance with a first wireless communications protocol of a first wireless communications system;

configuring a baseband co-processor of a multi-mode device to operate in accordance with a second wireless communications protocol of a second wireless communications system; and

establishing, within said device, timing synchronization between said first and second communication systems on the basis of timing information transferred to said host baseband processor from said baseband co-processor.

10. The method of claim 9, wherein said establishing includes issuing a timer capture interrupt to said baseband co-processor.

11. The method of claim 10, wherein said establishing comprises providing at least one timer value pertinent to a timing state of said second wireless communications

system to said host baseband processor in response to issuance of said timer capture interrupt.

12. The method of claim 9, wherein said establishing includes reading a current value of at least one timer maintained by said baseband co-processor consistent with said second wireless communications protocol.

13. The method of claim 11, wherein said second wireless communications protocol comprises WCDMA, said establishing including storing at least one timer value and an additional timer value pertinent to an additional timing state of said second wireless communications system in first and second registers of said baseband co-processor.

14. The method of claim 9, wherein said host baseband processor is configured to effect higher-layer processing of information processed by said baseband co-processor.

15. A method for wireless communication, the method comprising:

generating within a multi-mode communication device, a timer capture interrupt during a predetermined timing phase of a first wireless communication system, wherein said multi-mode communication device communicates via a first wireless protocol with said first wireless communication system, and said multi-mode communication device

communicates via a second wireless protocol with a second wireless communication system;

storing a timer value of at least one time pertinent to operation of said second wireless communication system in response to said timer capture interrupt;

reading said timer value; and

determining a timing relationship between said first and second wireless communication systems based upon said timer value.

16. The method of claim 15, comprising:

storing an additional timer value of at least one other timer pertinent to operation of said second wireless communication system in response to said timer capture interrupt; and

reading said additional timer value, said timing relationship being based at least in part upon said additional timer value.

17. The method of claim 15, wherein one or more timers are incremented pursuant to operation of said first wireless communication system, said determining a timing relationship including comparing at least one value of said one or more timers with said timer value.

18. The method of claim 15, wherein said first wireless communications system operates in accordance with a first wireless communications protocol, and said second wireless communications system operates in accordance with a second wireless communications protocol different from said first wireless communications protocol.

19. The method of claim 18, wherein said first wireless communications protocol comprises GSM, and said second wireless communications protocol comprises WCDMA.

20. A multi-mode wireless communication device, comprising:

a host baseband processor configured to operate in accordance with a first wireless communications protocol of a first wireless communications system; and

a baseband co-processor configured to operate in accordance with a second wireless communications protocol of a second wireless communications system,

wherein one or more of said host baseband processor, said baseband co-processor and/or additional circuitry, enables timing synchronization between said first and second wireless communications systems on the basis of timing information transferred to said host baseband processor from said baseband co-processor.

21. The multi-mode communications device of claim 20, wherein said one or more of said host baseband processor, said baseband co-processor and/or said additional circuitry comprises circuitry for issuing, from said host baseband processor, a

timer capture interrupt to said baseband co-processor during a predetermined timer phase of said first wireless communications system.

22. The multi-mode communication device of claim 21, wherein said one or more of said host baseband processor, said baseband co-processor and/or said additional circuitry is configured to provide at least one timer value pertinent to a timing state of said second wireless communications system in response to issuance of said timer capture interrupt, said one or more of said host baseband processor, said baseband co-processor and/or said additional circuitry enables determining of a timing difference between said first and second wireless communication systems based upon said predetermined timer phase and said at least one timer value.

23. The multi-mode communications device of claim 21, wherein said one or more of said host baseband processor, said baseband co-processor and/or said additional circuitry comprises circuitry for reading a current value of at least one timer consistent with said second wireless communications protocol.

24. The multi-mode communications device of claim 20, wherein said host baseband processor comprises a higher-layer processing module and a modem for interfacing with said first wireless communication system, said higher-layer processing module being operatively coupled to said modem and to a baseband interface of said baseband co-processor.

25. The multi-mode communications device of claim 22, wherein said second wireless communications protocol comprises WCDMA, said one or more of said host baseband processor, said baseband co-processor and/or said additional circuitry including first and second registers adapted to store said at least one timer value and an additional timer value pertinent to said second wireless communications protocol.

26. The multi-mode communications device of claim 25, wherein said at least one timer value corresponds to a slot counter and said additional timer value corresponds to a sample counter.

27. Multi-mode communications device of claim 20, wherein said host baseband processor comprises a higher-layer processor configured to effect higher-layer processing of information processed by said baseband co-processor.

28. A multi-mode wireless communication device, comprising:

a host baseband processor configured to operate in accordance with a first wireless communications protocol of a first wireless communications system; and

a baseband co-processor configured to operate in accordance with a second wireless communications protocol of a second wireless communications system,

wherein said host baseband processor enables timing synchronization between said first and second wireless communications systems on the basis of timing information transferred to said host baseband processor from said baseband co-

processor, wherein said host baseband processor comprises circuitry for issuing, from said host baseband processor, a timer capture interrupt to said baseband co-processor during a predetermined timer phase of said first wireless communications system, and wherein said baseband co-processor is configured to provide at least one timer value pertinent to a timing state of said second wireless communications system to said host baseband processor in response to issuance of said timer capture interrupt, said host baseband processor enables determining of a timing difference between said first and second wireless communication systems based upon said predetermined timer phase and said at least one timer value.

29. The multi-mode communications device of claim 28, wherein said host baseband processor comprises circuitry for reading a current value of at least one timer maintained by said baseband co-processor consistent with said second wireless communications protocol.

30. The multi-mode communications device of claim 28, wherein said host baseband processor comprises a higher-layer processing module and a modem for interfacing with said first wireless communication system, said higher-layer processing module being operatively coupled to said modem and to a baseband interface of said baseband co-processor.

31. The multi-mode communications device of claim 28, wherein said second wireless communications protocol comprises WCDMA, said baseband co-processor

including first and second registers adapted to store said at least one timer value and an additional timer value pertinent to said second wireless communications protocol.

32. The multi-mode communications device of claim 31, wherein said at least one timer value corresponds to a slot counter and said additional timer value corresponds to a sample counter.

33. The multi-mode communications device of claim 28, wherein said host baseband processor comprises a higher-layer processor configured to effect higher-layer processing of information processed by said baseband co-processor.

34. A timing synchronization method, comprising:

configuring a host baseband processor of a multi-mode device to operate in accordance with a first wireless communications protocol of a first wireless communications system;

configuring a baseband co-processor of a multi-mode device to operate in accordance with a second wireless communications protocol of a second wireless communications system; and

establishing, within said device, timing synchronization between said first and second communication systems on the basis of timing information transferred to said host baseband processor from said baseband co-processor, wherein said establishing includes issuing a timer capture interrupt to said baseband co-processor, and wherein

said establishing comprises providing at least one timer value pertinent to a timing state of said second wireless communications system to said host baseband processor in response to issuance of said timer capture interrupt.

35. The method of claim 34, wherein said establishing includes reading a current value of at least one timer maintained by said baseband co-processor consistent with said second wireless communications protocol.

36. The method of claim 34, wherein said second wireless communications protocol comprises WCDMA, said establishing including storing at least one timer value and an additional timer value pertinent to an additional timing state of said second wireless communications system in first and second registers of said baseband co-processor.

37. The method of claim 34, wherein said host baseband processor is configured to effect higher-layer processing of information processed by said baseband co-processor.

38. A multi-mode wireless communication device, comprising:

a host baseband processor configured to operate in accordance with a first wireless communications protocol of a first wireless communications system; and

a baseband co-processor configured to operate in accordance with a second wireless communications protocol of a second wireless communications system,

wherein one or more of said host baseband processor, said baseband co-processor and/or additional circuitry, enables timing synchronization between said first and second wireless communications systems on the basis of timing information transferred to said host baseband processor from said baseband co-processor, wherein said one or more of: said host baseband processor, said baseband co-processor and said additional circuitry comprises circuitry for issuing, from said host baseband processor, a timer capture interrupt to said baseband co-processor during a predetermined timer phase of said first wireless communications system, and wherein said one or more of said host baseband processor, said baseband co-processor and/or said additional circuitry is configured to provide at least one timer value pertinent to a timing state of said second wireless communications system in response to issuance of said timer capture interrupt, said one or more of said host baseband processor, said baseband co-processor and/or said additional circuitry enables determining of a timing difference between said first and second wireless communication systems based upon said predetermined timer phase and said at least one timer value.

39. The multi-mode communications device of claim 38, wherein said one or more of said host baseband processor, said baseband co-processor and/or said additional circuitry comprises circuitry for reading a current value of at least one timer consistent with said second wireless communications protocol.

40. The multi-mode communications device of claim 38, wherein said host baseband processor comprises a higher-layer processing module and a modem for

interfacing with said first wireless communication system, said higher-layer processing module being operatively coupled to said modem and to a baseband interface of said baseband co-processor.

41. The multi-mode communications device of claim 38, wherein said second wireless communications protocol comprises WCDMA, said one or more of said host baseband processor, said baseband co-processor and/or said additional circuitry including first and second registers adapted to store said at least one timer value and an additional timer value pertinent to said second wireless communications protocol.

42. The multi-mode communications device of claim 41, wherein said at least one timer value corresponds to a slot counter and said additional timer value corresponds to a sample counter.

43. The multi-mode communications device of claim 38, wherein said host baseband processor comprises a higher-layer processor configured to effect higher-layer processing of information processed by said baseband co-processor.

EVIDENCE APPENDIX
(37 C.F.R. § 41.37(c)(1)(ix))

(1) USPP 2002/0141441 ("Neumann", entered into record by the Examiner in the December 11, 2008 Final Office Action.

(2) USP 5,918,040 ("Jarvis"), entered into record by the Examiner in the December 11, 2008 Final Office Action.

(3) USPP 2002/0186754 ("Kawai"), entered into record by the Examiner in the December 11, 2008 Final Office Action.

RELATED PROCEEDINGS APPENDIX
(37 C.F.R. § 41.37(c)(1)(x))

The Appellant is unaware of any related appeals or interferences.